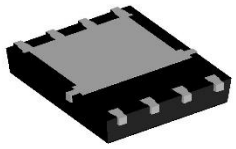
SNM105R3DNA

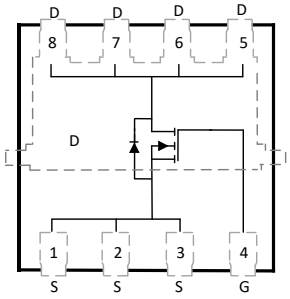
Single N-Channel, 100V, 95A, Power MOSFET

http://www.sitcores.com/

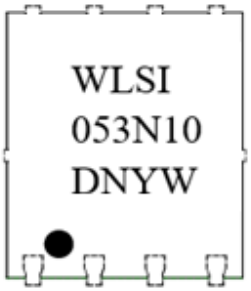
V_{DS} (V)	Max.$R_{DS(on)}$ (mΩ)
100	5.3 @ V_{GS}=10V
	7.7 @ V_{GS}=4.5V



PDFN5X6-8L



Pin configuration (Top view)



WLSI	=Company (Group) Code
053N10	=Device Code
DN	=Special Code
Y	=Year
W	=Week(A~z)

Marking

Description

The SNM105R3DNA is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product SNM105R3DNA is Pb-free.

Features

- Trench Technology
- Supper high density cell design
- Low ON resistance
- Low Threshold Voltage
- Package PDFN5X6-8L

Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
SNM105R3DNA-8/TR	PDFN5X6-8L	5000/Tape&Reel

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_C=25°C	I_D	95	A
	T_C=100°C		63	A
Pulsed Drain Current [c]		I_{DM}	300	A
Continuous Drain Current	T_A=25°C	I_{DSM}	28	A
	T_A=70°C		22	
Avalanche Energy L=0.3mH		E_{AS}	220	mJ
Power Dissipation [b]	T_C=25°C	P_D	99	W
	T_C=100°C		40	
Power Dissipation [d]	T_A=25°C	P_{DSM}	7.7	W
	T_A=70°C		4.9	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance [a]	t ≤ 10 s	$R_{\theta JA}$	13	16	°C/W
	Steady State		39	47	
Junction-to-Case Thermal Resistance	Steady State	$R_{\theta JC}$	0.9	1.3	

Note:

a FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) partially covered with copper (645mm^2 area).

b The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial TJ =25°C, the maximum allowed junction temperature of 150°C.

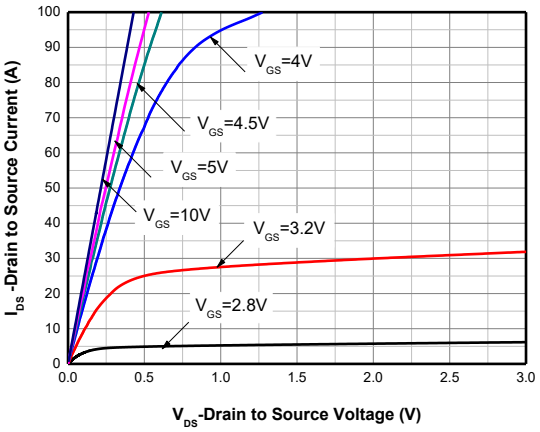
d The power dissipation P_{DSM} is based on Junction-to-Ambient thermal resistance $R_{\theta JA}$ t≤10s value and the $T_{J(MAX)}$=150°C.

e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

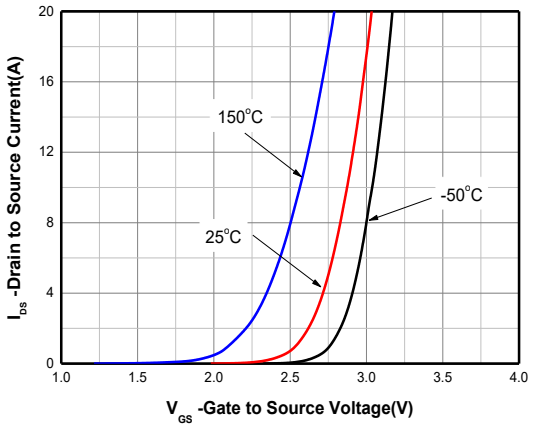
Electronics Characteristics (Ta=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250uA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V			1	μA
Gate-to-source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250uA	1.5	2.0	2.5	V
Drain-to-source On-resistance	$R_{DS(on)}$	V_{GS} =10V, I_D = 20A		4.3	5.3	mΩ
		V_{GS} = 4.5V, I_D = 20A		5.7	7.7	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0V, f = 1.0MHz, V_{DS} = 50 V		4000		pF
Output Capacitance	C_{OSS}			720		
Reverse Transfer Capacitance	C_{RSS}			20		
Total Gate Charge	$Q_{G(10V)}$	V_{GS} = 10 V, V_{DD} = 50V, I_D = 20A		77		nC
Total Gate Charge	$Q_{G(4.5V)}$			42		
Gate-to-Source Charge	Q_{GS}			13		
Gate-to-Drain Charge	Q_{GD}			20		
Gate Resistance	R_g	F = 1MHz		0.8		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$td_{(ON)}$	V_{GS} = 10 V, V_{DD} = 50 V, R_L = 2.5 Ω , R_G = 3Ω		12		ns
Rise Time	tr			20		
Turn-Off Delay Time	$td_{(OFF)}$			50		
Fall Time	tf			22		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 1A		0.7	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=20A,di/dt=100A/us		49		ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=20A,di/dt=100A/us		96		nC
Maximum Continuous Current	Is				80	A

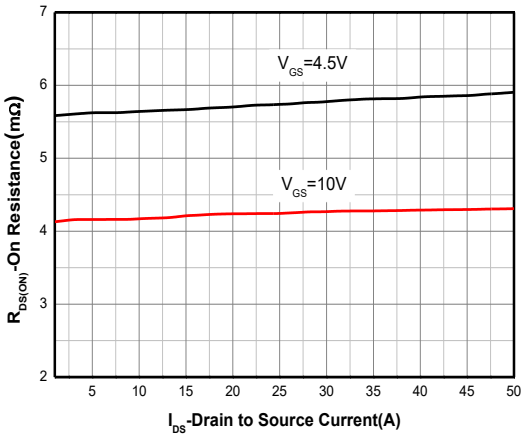
Typical Characteristics (Ta=25°C, unless otherwise noted)



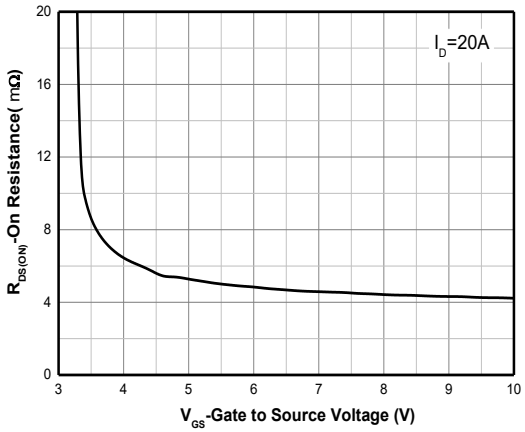
Output Characteristics[e]



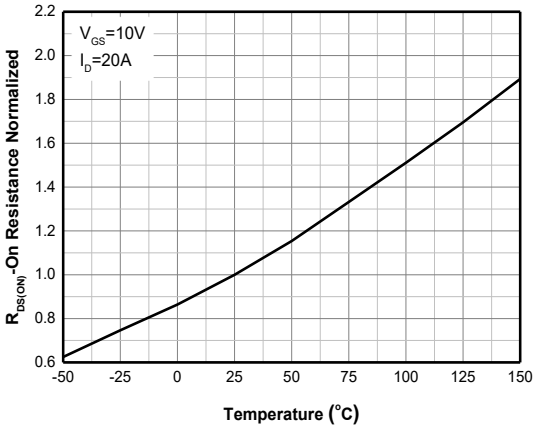
Transfer Characteristics[e]



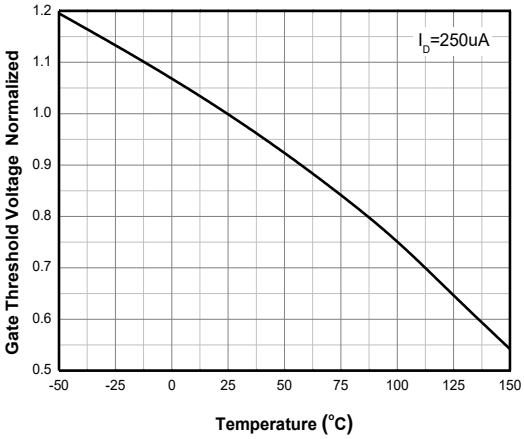
On-Resistance vs. Drain Current[e]



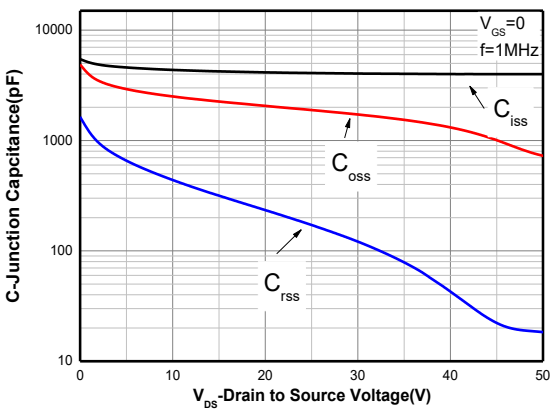
On-Resistance vs. Gate-to-Source Voltage[e]



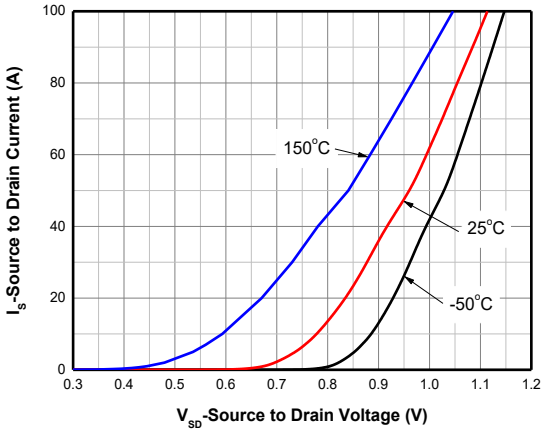
On-Resistance vs. Junction Temperature[e]



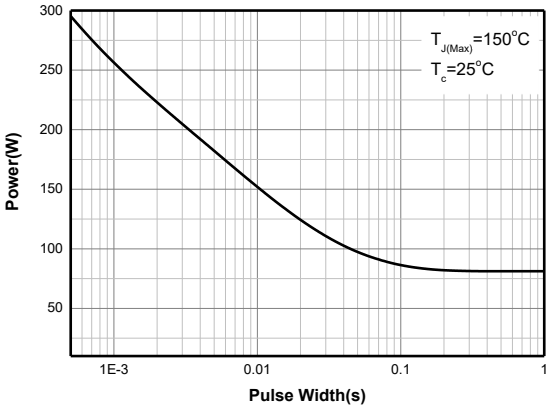
Threshold Voltage vs. Temperature[e]



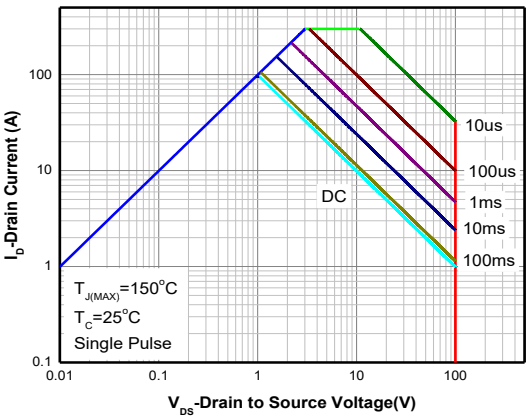
Capacitance



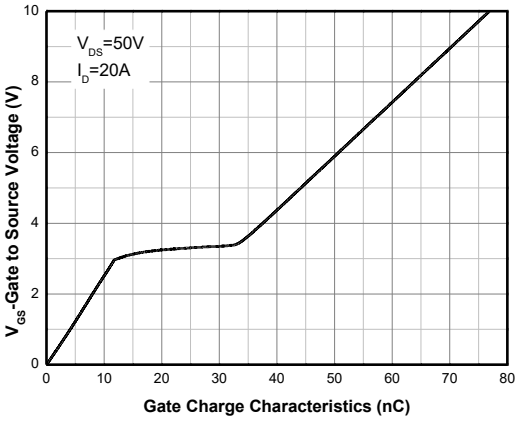
Body Diode Forward Voltage[e]



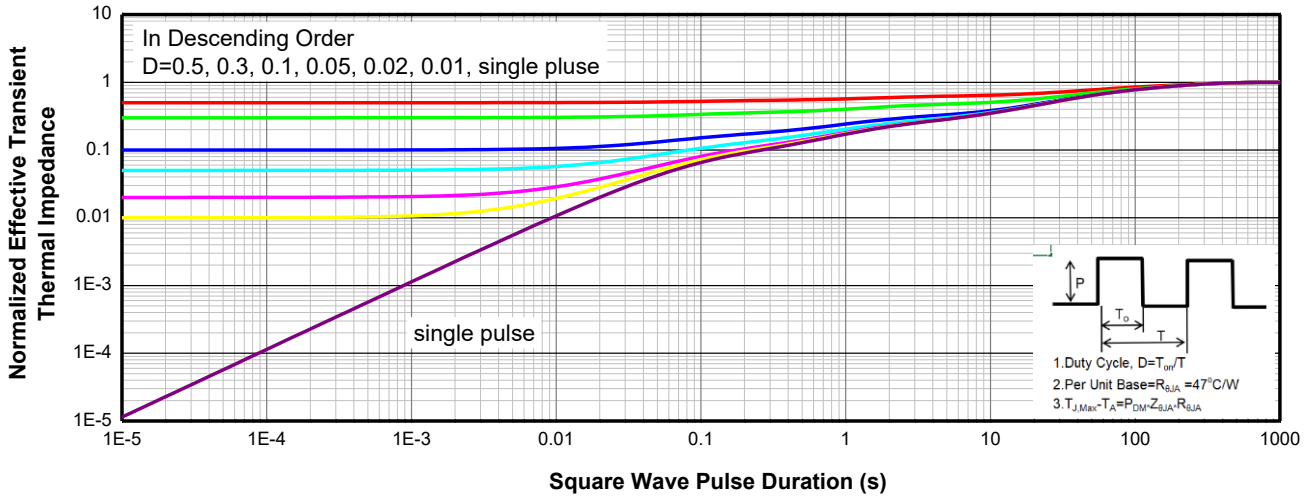
Single Pulse power



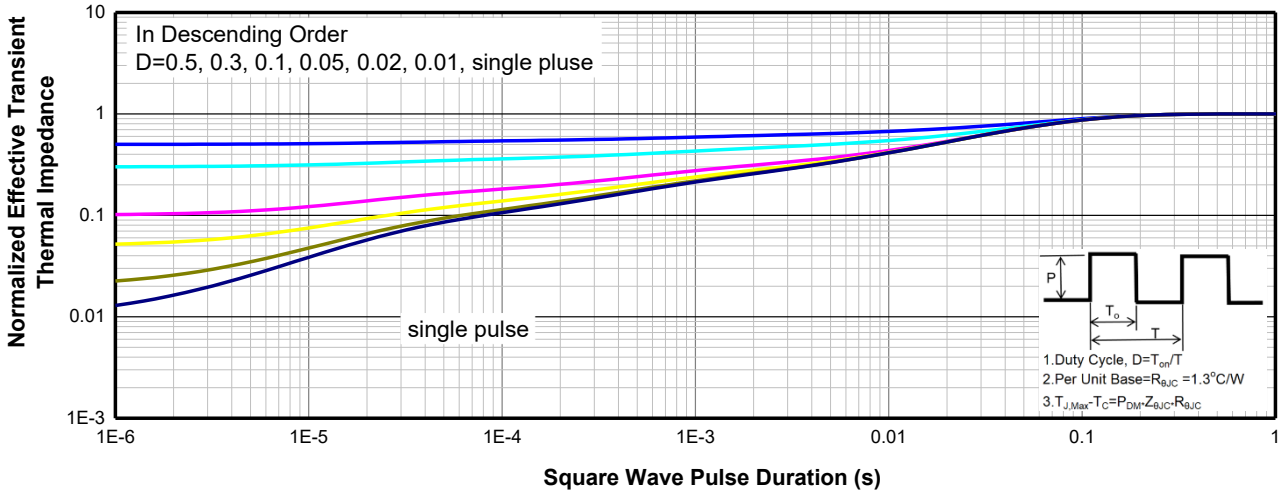
Safe Operating Area



Gate Charge Characteristics



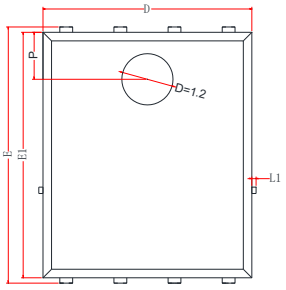
Transient Thermal Response (Junction-to-Ambient)



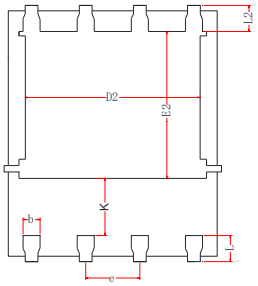
Transient Thermal Response (Junction-to-Case)

PACKAGE OUTLINE DIMENSIONS

PDFN5x6-8L

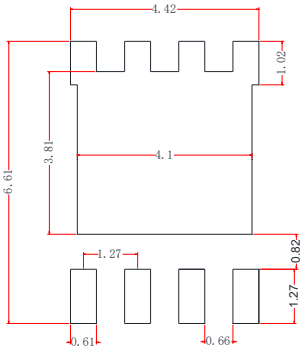


TOP VIEW



BOTTOM VIEW

SIDE VIEW

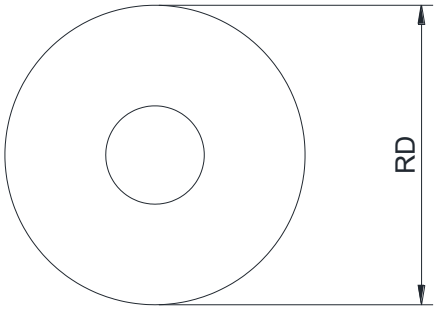


RECOMMENDED LAND PATTERN(Unit:mm)

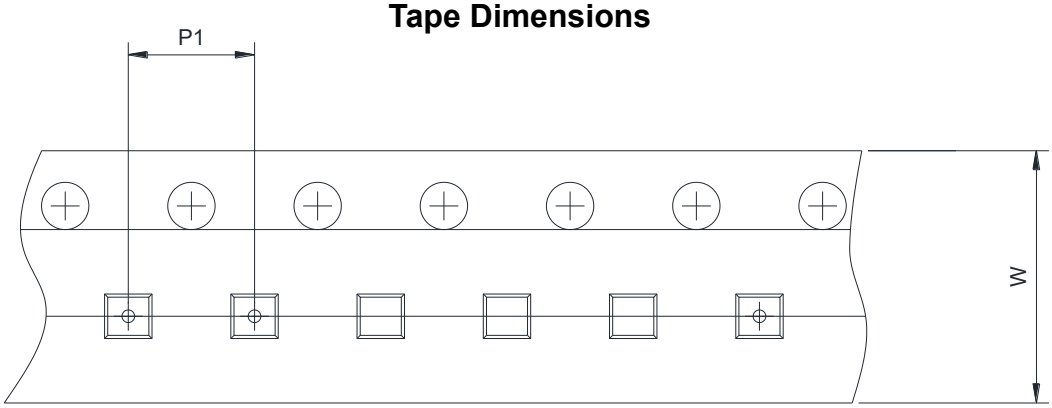
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	1.00	1.10	1.20
b	0.35	0.40	0.45
c	0.21	0.25	0.34
D	4.80	4.90	5.00
D2	3.82	-	4.11
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.18	-	3.54
e	1.27BSC		
K	1.10	-	-
L	0.51	0.61	0.71
L1	-	-	0.10
L2	0.51	0.61	0.71
P	1.00	1.10	1.20
θ	8°	-	12°

TAPE AND REEL INFORMATION

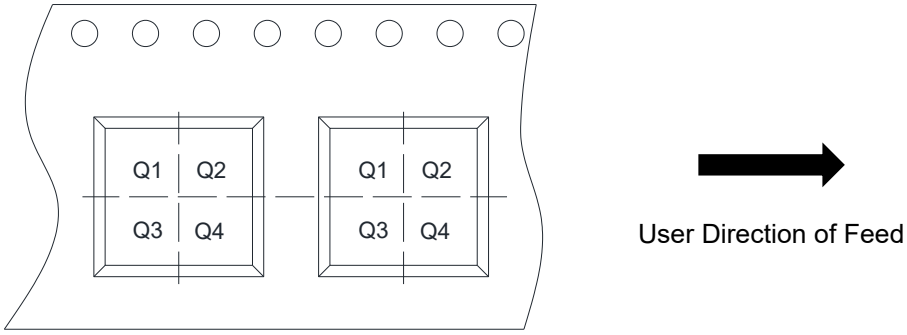
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch	☑ 13inch		
W	Overall width of the carrier tape	☐ 8mm	☑ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☐ 4mm	☑ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4